**Curriculum Vitae**

**Dr. Pranab Roy**

**Assistant Professor**

School of VLSI Technology

Indian Institute of Engineering Science and Technology, Shibpur

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**Permanent Address**

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Kolkata – 700012

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**Objective**

To work with a reputed institution as an Associate professor/Senior Assistant professor, where my acquired technical skills and knowledge will be utilized towards imparting quality education and research, other diverse job responsibilities, continuous growth and contribution to the Institution success.

**Personal skills**

* Good communication and writing skills.
* Profound knowledge in the areas of VLSI Design automation and Information Technology.
* Excellent in providing real time knowledge for the students.
* Strong analytical, logical and mathematical skills.
* Ability to conduct independent research and guide students for post graduate dissertations.
* Good Presentation, motivational and leadership qualities.

**Educational Qualifications**

*Ph. D -* Awarded, Department of Information Technology, I.I.E.S.T, Shibpur, 2016

 *Thesis* – Design Automation for Digital Microfluidic Biochips: Droplet Routing,

 Wire Planning and Detection Mechanism. .

*M.Tech -* **Information Technology**, Purabi Das School of Information Technology,

 Bengal Engineering and Science University, Shibpur, (currently I.I.E.S.T, Shibpur)2007, CGPA -9.61.(1st Class). [Ranked 1st]

*A.M.I.E* - **Electronics and Communication** Engineering (Section B) [Additional

 Engineering Qualification], Institution of Engineers, India, 2001, 60.4%

 (1st Class). [Ranked 1st from West Bengal state centre]

*B.E -* **Marine** Engineering (graduation) , DMET ,Calcutta(currently Indian Maritime

 University, Kolkata), 1989, 61% (1st Class).

*Higher Secondary* - Hindu School, Calcutta (West Bengal Council of Higher Secondary

 Education), 1984, 55% (2nd Division).

*Secondary* - Hindu School, Calcutta (West Bengal Board of Secondary Education), 1982,

 72.3 % (1st Division), State rank 134. (Awarded merit scholarship).

**Current Position**

***Assistant Professor (contractual)* ,** School of VLSI Technology, Indian Institute of Engineering Science and Technology, Shibpur, Howrah (April 2012 – till date).

**Academic Experience**

* ***Visiting Faculty***, M.Tech (Microelectronics and VLSI Technology),MAKAUT, WB, India(March,2018 – August,2018)
* ***Visiting Faculty,*** M.Sc(Computer Science),Ashutosh College(affiliated to Calcutta University),WB(August,2016 – Till date).
* ***Visiting Faculty***, M.Tech (Biomedical Engineering), Centre for healthcare technology, I.I.E.S.T, Shibpur (January,2018 – Till Date).
* ***Visiting Faculty***, B.Tech (CS/I.T), Indian Institute of Information Technology, Kalyani, Nadia, West Bengal (April 2016 – December 2017).
* ***Visiting Faculty***, M.Tech (I.T), Purabi Das School of Information Technology, I.I.E.S.T, Shibpur, Howrah (August 2007 – December, 2015).
* ***Visiting Faculty***, B.E (I.T), Department of Information Technology, Bengal Engineering and Science University, Shibpur, Howrah (August 2007 – May, 2013).
* ***Visiting Faculty*,** PGD (Bioinformatics), Purabi Das School of Information Technology, I.I.E.S.T, Shibpur, Howrah (August 2005 – April 2008).
* ***Project Faculty***, School of VLSI Technology, Bengal Engineering and Science University, Shibpur, Howrah (September 2010– April, 2012).
* ***Laboratory/Research Engineer*** - School of VLSI Technology, Bengal Engineering and Science University, Shibpur, Howrah (January 2007– September, 2010).

Total academic experience (post M.Tech) – 8.75 years (faculty) + 3.75 years (Laboratory Engineer) [Post PhD – 3.25 years]

**Industrial Experience**

* *Senior Marine Engineer Officer*, **Poompuhar Shipping Corporation Ltd.** (Govt. of Tamilnadu) from August, 2001 to April, 2003.
* *Marine Engineer officer*, **ESSAR Shipping Ltd.** from March, 1998 to January, 1999.
* *Junior Marine* ***Engineer Officer*, ESSAR SISCO Ship management Co.Ltd.** from December ,1995 to November ,1996.
* *Junior Marine Engineer Officer,* **Shipping Corporation of India** from March 1990 to October, 1990.

**Academic Responsibilities**

* Taken independent responsibility of conducting courses on different subjects for M.Tech and B.E level at I.I.E.S.T ,Shibpur (formerly B.E.S.U, Shibpur)
* Taken responsibility as head examiner for arrangement and conducting of semester examination for M.Tech courses of all 5 semesters (till date)at School of VLSI Technology, IIEST, Shibpur for last 2 years.
* Taken the role as convenor of Departmental Faculty Academic Committee for last 7.5 years.
* Conducted laboratory sessions and preparation of assignments for development of technical skills followed by evaluation and guidance of students.
* Supervised M.E/M.Tech projects for P.G students in the areas of VLSI Design and Information Technology.
* Installation and upgradation of EDA tools and maintenance of laboratory equipments (FPGA and ASIC design laboratories).
* Conducted research in different areas and helping other P.G and Ph. D students to prepare technical research papers for publication at different journal and conferences
* Conducted different summer training programs to confer specialized education in specified areas to students and teachers of other institutions.
* Helped senior professors and colleagues to prepare tutorials and other technical excerpts for students.
* Handled project related activities namely preparation of project reports, utilization certificates and other project administration issues.
* Attended seminars, workshops and Instruction Enhancement programs (IEP) for exploring new areas for research and enhancement of knowledge.
* Presented tutorials and research papers at different conferences in India and abroad.
* Current member of Departmental Training and Placement Committee from current semester onwards.
* Member and secretary of Departmental Purchase Committee.

**Laboratory Experience:**

* Set up VLSI Design Laboratory at School of VLSI Technology ,IIEST,Shibpur
* Installed EDA tools namely Cadence, Synopsys, Mentor graphics, CoWare and Magma
* Installed FPGA tools (Xilinx ISE 14.1 and Vivado suites)at both VLSI and IT Labs at IIEST,Shibpur
* Developed FPGA board level designs using Spartan 3E,Virtex 2 pro,Virtex 4 and Virtex 7 FPGA boards at School of VLSI technology, IIEST, Shibpur
* Currently developing embedded systems laboratory at school of VLSI Technology using Arduino Uno, Arduino Mega and Raspberry pi 3 devices with requisite accessories.
* Taken laboratory classes for Digital VLSI design using VHDL for M.Tech(VLSI design) at School of VLSI technology, IIEST, Shibpur.
* Taken laboratory classes for Object oriented programming using C++ for B.E(IT) at Department of Information Technology, BESU,Shibpur (currently IIEST, Shibpur)
* Responsible for setting up of UML and OOP laboratory at PDSIT, IIEST,Shibpur .
* Taken laboratory classes for Object oriented programming methodology using c++ and Java for M.Tech(IT) at PDSIT, IIEST, Shibpur
* Taken responsibility for setting up of FPGA laboratory for Computer Architecture [B.Tech(IT)]at IIIT, Kalyani.
* Taken laboratory classes for Computer Organization and Computer Architecture [B.Tech(IT) and B.Tech(CS)] at IIIT, Kalyani.
* Taken responsibility for setting up of Embedded systems(Arduino) laboratory for Microcontrollers and Embedded Systems [B.Tech(IT)]at IIIT, Kalyani.

**List of courses taught**

1. VLSI Physical Design – M.Tech(VLSI Design) – (2010-till date) (PG)
2. Computer Systems Architecture - M.Tech(VLSI Design),M.Tech(Information and Communication Technology) – (2010- till date) (PG)
3. System on Chip and Test - M.Tech(VLSI Design) – (2012-till date) (PG)
4. Digital VLSI Design – M.Tech(VLSI Design) – (2019-till date) (PG)
5. Logic Synthesis and Verification – M.Tech(VLSI Design) – (2018-till date) (PG)
6. Object Oriented Systems - M.Tech(IT) – (2007-2015) (PG)
7. Embedded Systems – M.Tech(IT) –(2010-2012) –(PG)
8. Computer organization – B.Tech (CS/IT) – (2016- till date) (UG)
9. Computer Architecture - B.Tech (IT) – (2016- till date) (UG)
10. Object Oriented Programming Methodology - B.Tech(IT) – (2007-2014) (UG)
11. CAD for VLSI - B.Tech(IT) – (2013) (UG)
12. Microcontrollers – B.Tech(CS/IT) – (2017 – till date) (UG)
13. Embedded Systems – B.Tech(CS/IT) –(2017-Till date) (UG)
14. Microfluidics and Nanofluidics – M.Tech(Biomedical Engineering) – (2018 – till date)(PG)
15. Advanced Computer Architecture – M.Sc (Computer Science) –(2016 – till date)(PG)
16. VLSI Design - M.Sc (Computer Science) –(2016 – till date)(PG)

**Doctoral Research (Brief description)**

Early research on CAD for digital microfluidic based biochips has been focused on device-level physical modelling of single component. As the use of digital microfluidic based biochips increases, their complexity is expected to become significant due to the need for multiple and concurrent assays on the chip, as well as more sophisticated control for resource management.

 The research contributes to the area of design automation and testing of Digital Microfluidic Biochips followed by development of automated detection mechanism and its cyber physical application targeted towards the development of an integrated biochip system.

* To develop new techniques for geometrical synthesis and chip level wire planning to enhance performance for Bioassay execution in Digital microfluidic biochips.
* To develop new testing methodologies for DMFB towards efficient planning of test schedule resulting in minimal and efficient utilization of test resources with optimal test completion time.
* To develop automated detection mechanism for detection analysis and efficient cyber- physical application using multiple biochips for intelligent medical diagnostic application.

**Area of Research Interest**

* **Digital Microfluidics**
* **VLSI Physical Design**
* **Computational Intelligence**
* **Cognitive Computing**
* **Cyberphysical systems**
* **Embedded Systems and Architecture**
* **Algorithms and Data Structures**

 **Avocation**

* **Creative Writing**
* **Sketching**
* **Reading**
* **Singing**

**Language Proficiency**

* **English**
* **Hindi**
* **Bengali**
* **German**

**Experience on VLSI Design and Related Areas**

1. Worked as Research engineer under SMDP II project – responsible for installation and maintenance of VLSI EDA tools and development of FPGA laboratory.
2. Participated in India chip design program and involved in design of VLSI Chips (Total four in number), in collaboration with IISc, Bangalore , IIT, Kharagpur, NIT , Surathkal and PSG ,Coimbatore.
3. Organized summer training and workshops on ASIC Design flow at IIEST, Shibpur
4. Currently involved in developing a controller chip for intelligent traffic control system. (FPGA prototype is already developed).
5. Expertise on Synopsis EDA tools (both front and back end flow) for Digital VLSI Design.

**Publications**

**International Journals**

#### Pampa Howladar,**Pranab Roy**,Hafizur Rahaman ,” A High-Performance Droplet Routing Technique for MEDA Based Biochips”, ACM Journal on Emerging Technology in Comuting (Accepted)(SCI Indexed;IF – 1.672).

#### Pampa Howladar,**Pranab Roy**,Hafizur Rahaman,“ Design Automation and Testing of MEDA Based Digital Microfluidic Biochips: A Brief Survey.”,IETE Journal of Research ,Taylor and Francis.(Accepted)( SCI Indexed ;IF – 0.793)

#### Rupam Bhattacharya, **Pranab Roy**,Hafizur Rahaman,“ Homogeneous Droplet Routing in DMFB: An Enhanced Technique for High Performance Bioassay Implementation” ElsevierVLSI Integration ,2018,Vol 60,pp.74-91.(SCI Indexed ; IF – 1.153).

#### **Pranab Roy**,Swati Saha,Hafizur Rahaman,Parthasarathi Dasgupta,“ Novel Wire Planning Schemes for Pin Minimization in Digital Microfluidic Biochips ”- IEEE Transactions on Very Large Scale Integration Systems ,volume 24,issue 11,November,2016, pp.3245-3358.(SCI Indexed ,IF – 1.946)

#### **Pranab Roy**, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html) ,“Two-level clustering-based techniques for intelligent droplet routing in digital microfluidic biochips. ”Elsevier [Integration Volume 45](http://www.informatik.uni-trier.de/~ley/db/journals/integration/integration45.html#RoyRD12), issue3: 316-330 (2012). (SCI Indexed ,IF – 1.153)

#### Nachiketa Das, **Pranab Roy** and Hafizur Rahaman, “ BIST For Testing And Diagnosis Of Delay Fault in Cluster Based Field Programmable Gate Arrays.” IET Journal of Computers & Digital Techniques, vol-7,issue 5, Sept. 2013, pp-210-222(SCI Indexed ,IF – 0.515)

####  Nachiketa Das, **Pranab Roy** and Hafizur Rahaman, “Bridging Fault Detection in Cluster Based FPGA by Using Muller-C Element .” Elsevier Journal of Computer and Electrical Engineering vol-39, 2013, pp-225-236. (SCI Indexed ,IF – 1.570).

#### Rupam Bhattacharyay, **Pranab Roy**,Hafizur Rahaman,” A complete routing simulator for digital microfluidic biochip“ **International Journal of Information System Modeling and Design, International Journal of Information System Modeling and design**  , **IGI Global,vol- 10,issue -2,2019,pp-70-85 (Scopus indexed)**

#### Nachiketa Das, **Pranab Roy** and Hafizur Rahaman, “Detection of Crosstalk Faults in Field Programmable Gate Arrays (FPGA). ” published in [Journal of The Institution of Engineers (India): Series B](http://link.springer.com/journal/40031)  IEI(B) (Springer), vol 96(issue 3), July 2014, pp.227-236(Scopus Indexed).

#### Debnath Bhattacharyya, Arpita Roy, **Pranab Roy** and Tai-hoon Kim,“ Receiver Compatible Data Hiding in Color Image”, International Journal of Advanced Science and Technology, volume 6, May, 2009,pp 15-24. (Scopus Indexed).

**International Conferences**

#### Pampa Howladar, **Pranab Roy**, Hafizur Rahaman,“ Micro-electrode-dot array based Biochips : Advantages of  Using Different Shaped CMAs ” , IEEE Computer Society Annual Symposium on VLSI(ISVLSI),2019 ,North Miami,Florida,USA (accepted)

#### Pampa Howladar, **Pranab Roy**, Subhajit Chatterjee, Hafizur Rahaman, “Daisy Chain Based Actuation Techniques for MEDA Based Biochips: A Detailed Analysis”,6th International Conference on Computing, Communication and Sensor Network ,2018,Kolkata.

#### Rupam Bhattacharya, **Pranab Roy** and Hafizur Rahaman,“ A New Homogeneous Droplet Transportation Algorithm and Its Simulator to Boost Route Performance in Digital Microfluidic Biochips” Proceedings of IEMIS,Vol 1,2018 ,Advances in Intelligent Systems and Computing,Springer ,issue 755.

#### Rupam Bhattacharya, **Pranab Roy** and Hafizur Rahaman,” A New Combined Routing Technique in Digital Microfluidic Biochip,” Proceedings of IEMIS,Vol 1,2018 ,Advances in Intelligent Systems and Computing,Springer ,issue 755.

#### Arindam Sinha Roy, Subrata Das, **Pranab Roy**, Hafizur Rahaman,“ An Angular Steiner Tree Based Global Routing Algorithm For Graphene Nanoribbon Circuit”, 22ND VLSI Design and Test Symposium (VDAT-2018), Madurai,India.2018(accepted)

#### **Pranab Roy**, Habibur Rahaman ,“Bioassay -Protocol to Layout:A DMFB Based Implementation”Proc. of 1st IEEE International Symposium on Devices,Circuits and Systems,2018,IIEST,Shibpur,India (accepted).

#### Arindam Sinharoy, **Pranab Roy**, Hafizur Rahaman,“ Computing Fréchet Distance Metric based L-Shape Tile Decomposition for E-Beam Lithography”, Proc. of 31th IEEE International conference of VLSI Design,2018,Pune,India. Pp. 313-318.

#### **Pranab Roy**, Amiya Sahoo,Hafizur Rahaman,“ Adaptive Medical Detection System: An Iterative Averaging Method for Automated Detection Analysis using DMFBs ”,Proc. of 7th IEEE International Symposium on Embedded Computing and Systems Design, 2017,Durgapur,India pp.1-6.

#### Arindam Sinharoy, **Pranab Roy**, Hafizur Rahaman ,“ Hausdorff Distance Driven L-shape Matching Based Layout Decomposition for E- Beam Lithography” , 21st VLSI Design and Test Symposium 2017,Roorkee,Springer CCIS ,Vol 711,pp. 287-295.

#### Arindam Sinharoy, **Pranab Roy**, Hafizur Rahaman,”VLSI Thermal Placement issues:A cooperative game theory based approach”,6 th IEEE International Symposium on Embedded Computing and Systems Design,Patna,2016,pp.106-111.

#### Pampa Howladar,**Pranab Roy**,Hafizur Rahaman,“ An Automated Design of Pin-Constrained Digital Microfluidic Biochip on MEDA Architecture” IEEE Fourth International Symposium on Women in Computing and Informatics (WCI-ICACCI,2016),Jaipur,India pp. 1565-1570.

#### Pampa Howladar, [Debashri Roy](http://dblp.uni-trier.de/pers/hd/r/Roy%3ADebashri), [**Pranab Roy**](http://dblp.uni-trier.de/pers/hd/r/Roy%3APranab), [Hafizur Rahaman](http://dblp.uni-trier.de/pers/hd/r/Rahaman%3AHafizur),“ **Cross-reference** EWOD driving scheme and cross-contamination aware net placement technique for MEDA based DMFBs.”,ICACCI,2016,Jaipur,India,pp. 614-619.

#### Arko Dutt,**Pranab Roy**,Hafizur Rahaman ,“ TSV-Aware 3-D IC Structural Planning with Irregular Die-Size” IEEE Asia Pacific Conference on Circuits & Systems,2016,Jeju,Korea, pp.713-716.

#### **Pranab Roy**, Sudeshna Chakraborty, Hafizur Rahaman ,“ Synthesis aware sample preparation techniques using random sample sets in DMFB”- Proc. of 20th IEEE International symposium on VLSI Design and Test ,2016,Guwahati,India,pp. 1-6.

#### **Pranab Roy**, Khokan Mondal,Mayuri Kundu,Hafizur Rahaman ,“ A New Sample Preparation Technique for Linear Dilution Gradient with Minimal Sample Utilization and Waste Generation in DMFBs ” - Proc, of 2nd IEEE conference on Electrical Information and Communication Technology ,2015, Khulna, Bangladesh.pp. 205-210

#### Rupam Bhattacharya,Hafizur Rahaman,**Pranab Roy**, “A new heterogeneous droplet routing technique and its simulator to improve route performance in Digital Microfluidic Biochips”,IEEE International conference on Microelectronics, Computing and Communication (Microcom), 2016, pp. 1-6.

#### **Pranab Roy**, Mriganka Chakrabarty, Aatreyi Bal, Hafizur Rahaman, Parthasarathi Dasgupta ,“ Decision-based Biochips: A Novel Design for Concurrent Executionof Networked Bioassays integrated in Scalable DMFBs “ – Proc, of 6th IEEE ASQED ,2015,Kualalampur,Malaysia .pp 138-143.

#### **Pranab Roy**, Pampa Howladar,Hafizur Rahaman,Parthasarathi Dasgupta ,“3D integration in biochips: New proposed architectures for 3D applications in ATDA based digital microfluidic biochips.”-Proc. of 10th IEEE DTIS Conference ,2015,Naples,Italy,pp.1-6.

#### **Pranab Roy**, Tamosa chakraborty, Hafizur Rahaman,Parthasarathi Dasgupta “Multilevel homogeneous detection analyzer for medical diagnostic application in Digital Microfluidic Biochips ”,Proc. of IEEE International symposium of electronic system design,Suratkal,2014.pp. 73-78.

#### **Pranab Roy,** Aatreyi Bal, Tamosa Chakraborty, Mriganka Chakraborty, Hafizur Rahaman, Parthasarathi Dasgupta,“ Optical detection in Biochips: A fuzzy based detection analyzer for homogeneous samples in DMFBs ” – Proc. of IEEE CYBER,Hongkong,China,2014.pp.551-556.

#### **Pranab Roy**, Samadrita Bhattacharya, Hafizur Rahaman, Parthasarathi Dasgupta ,“A new technique for layout based customized functional testing of modules in  Digital Microfluidic Biochips”,Proc. of IEEE EWDTS,2014,Kiev,Ukraine.pp.1-6.

#### **Pranab Roy**, Aatreyi Bal, Mahua Raha Patra, Hafizur Rahaman, Parthasarathi Dasgupta,“ Automated two stage detection and analyzer system in Multipartitioned Digital Microfluidic Biochips ”- Proc. of IEEE, ISCAS ,Melbourne, Australia, 2014. pp. 1836 -1840

####  [Indrajit Das](http://dblp.uni-trier.de/pers/hd/d/Das%3AIndrajit), [Manodipan Sahoo](http://dblp.uni-trier.de/pers/hd/s/Sahoo%3AManodipan), **Pranab Roy**, [Hafizur Rahaman](http://dblp.uni-trier.de/pers/hd/r/Rahaman%3AHafizur):,“A 45 uW 13 pJ/conv-step 7.4-ENOB 40 kS/s SAR ADC for digital microfluidic biochip applications. ”[VDAT 2014](http://dblp.uni-trier.de/db/conf/vdat/vdat2014.html#DasSRR14): pp.1-6

#### **Pranab Roy**,Hafizur Rahaman,Parthasarathi Dasgupta, “A layout based customized testing technique for total microfluidic operations in Digital Microfluidic Biochips”-Proc. of IEEE,DDECS,Warsaw,Poland,2014. pp. 122-128

#### **Pranab Roy**, Samadrita Bhattacharya,Rupam Bhattacharya,Firdousi Jamil Imam,Hafizur Rahaman,Parthasarathi Dasgupta ,“ A novel wire planning technique for optimum pin utilization in Digital Microfluidic Biochips ”–Proc. of 27th IEEE International conference of VLSI Design,2014,Mumbai,India.pp.510-515.

#### **Pranab Roy**, ,Aatreyi Bal, Mahua Raha Patra ,Hafizur Rahaman,Parthasarathi Dasgupta ,“ Feedback based automated detection analysis  in Digital Microfluidic Biochip Systems ”,-Proc. of IEEE International Conference on Control, Automation, Robotics and Embedded systems (CARE-2013),Jabalpur, India .pp. 1-6.

#### **Pranab Roy**, Mahua Raha Patra, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html),“An intelligent Biochip System for Diagnostic Process Flow based Integration of Combined Detection Analyzer”,-Proc. of IEEE ISED,Singapore ,December ,2013. pp. 108 -112.

#### **Pranab Roy**, Parthasarathi Gupta, Hafizur Rahaman, Parthasarathi Dasgupta,“A new customized testing technique using a novel design of droplet motion detector for digital microfluidic Biochip systems” – Proc of IEEE ICACCI, Mysore ,India,2013.pp. 897-902.

#### **Pranab Roy**,Rupam Bhattacharya,Pampa Howladar,Hafizur Rahaman,Parthasarathi Dasgupta,“A new cross contamination aware routing method with intelligent path exploration in Digital Microfluidic Biochips ”Proc. Of IEEE DTIS Conference 2013, Abu Dhabi,UAE.pp. 50-55.

#### **Pranab Roy**, Samadrita Bhattacharya, Rupam Bhattacharya, Hafizur Rahaman,Parthasarathi Dasgupta,“A new method for route based synthesis and placement in Digital Microfluidic Biochips ” Proc. Of VDAT , Springer CCIS, Jaipur ,India,2013.pp. 361-375.

#### **Pranab Roy**, Mahua Raha Patra, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html),“Digital Microfluidic System:A new design for heterogeneous sample based integration of multiple DMFBs ”Proc. of IEEE, ISCAS ,Beijing, China, 2013. pp. 1905-1909.

#### **Pranab Roy**, [Modud Sohid](http://www.informatik.uni-trier.de/~ley/pers/hd/s/Sohid%3AModud.html), [Sudipta Chakraborty](http://www.informatik.uni-trier.de/~ley/pers/hd/c/Chakraborty%3ASudipta.html), [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html),“[A new digital analyzer for optically detected samples in Digital Microfluidic Biochips](http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6292057&contentType=Conference+Publications&sortType%3Dasc_p_Sequence%26filter%3DAND%28p_IS_Number%3A6291930%29%26pageNumber%3D6) [”Proc. Of IEEE MWSCAS, Boise, Idaho, US,2012](http://dx.doi.org/10.1109/MWSCAS.2012.6292057) pp -462-465

#### **Pranab Roy**, [Modud Sohid](http://www.informatik.uni-trier.de/~ley/pers/hd/s/Sohid%3AModud.html), [Sudipta Chakraborty](http://www.informatik.uni-trier.de/~ley/pers/hd/c/Chakraborty%3ASudipta.html), [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html),“System on Biochips: A new design for integration of multiple DMFBs” Proc. Of IEEE ISED,Kolkata ,India,2012.pp.256-260.

#### **Pranab Roy**, Mahua Raha Patra, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html),“ A New design of a dual mode Bioassay detection analyzer for digital microfluidic biochips” Proc. Of IEEE CODIS 2012,Jadabpur, Kolkata,India ,pp. 310-313.

#### **Pranab Roy**, Mahua Raha Patra, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html), “ Novel designs of Digital detection analyzer for intelligent detectionand analysis in digital microfluidic Biochips” Proc. of IEEE IDT , Doha, Qatar 2012.pp.1-6.

#### **Pranab Roy**, Mahua Raha Patra, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html),“Automated parallel detection based analyzer System for integrated bioassays in Digital Microfluidic Biochips ” Proc of IEEE El Nano ,kiev,Ukraine 2012.pp. 310-315

#### **Pranab Roy**, [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html), [Bhargab B. Bhattacharya](http://www.informatik.uni-trier.de/~ley/pers/hd/b/Bhattacharya%3ABhargab_B%3D.html) ,“A New Look Ahead Technique for Customized Testing in Digital Microfluidic Biochips. ” Proc. of IEEE [ATS 2012](http://www.informatik.uni-trier.de/~ley/db/conf/ats/ats2012.html#RoyRDB12),Nigata,Japan: pp.25-30

#### **Pranab Roy**, [Rupam Bhattacharjee](http://www.informatik.uni-trier.de/~ley/pers/hd/b/Bhattacharjee%3ARupam.html), [Modud Sohid](http://www.informatik.uni-trier.de/~ley/pers/hd/s/Sohid%3AModud.html), [Sudipta Chakraborty](http://www.informatik.uni-trier.de/~ley/pers/hd/c/Chakraborty%3ASudipta.html), [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html) “An intelligent compaction technique for pin constrained routing in cross referencing digital microfluidic biochips.”- Proc. of ACM [CODES+ISSS 2012](http://www.informatik.uni-trier.de/~ley/db/conf/codes/codes2012.html#RoyBSCRD12),Tempere,Finland: pp.423-432

#### **Pranab Roy**, [Rupam Bhattacharjee](http://www.informatik.uni-trier.de/~ley/pers/hd/b/Bhattacharjee%3ARupam.html), [Hafizur Rahaman](http://www.informatik.uni-trier.de/~ley/pers/hd/r/Rahaman%3AHafizur.html), [Parthasarathi Dasgupta](http://www.informatik.uni-trier.de/~ley/pers/hd/d/Dasgupta%3AParthasarathi.html): A New Algorithm for Routing-Aware Net Placement in Cross-Referencing Digital Microfluidic Biochips. Proc. of IEEE [ISVLSI 2012](http://www.informatik.uni-trier.de/~ley/db/conf/isvlsi/isvlsi2012.html#RoyBRD12),Amherst,MS,US: pp. 320-325

#### **Pranab Roy,** Hafizur Rahaman, Parthasarathi dasgupta ,‘ Modelling, detection and diagnosis of multiple faults in Cross referencing DMFBs’,International conference on Informatics ,Electronics and Vision,Proc. Of IEEE ICIEV, 2012, Dhaka, Bangladesh.pp.1107-1112.

#### **Pranab Roy**, Hafizur Rahaman and P.S.Dasgupta,”A novel high performance routing technique for Cross-referencing DMFBs", Proc. Of IEEE International Conference on Biomedical Engineering (ICOBE 2012,Penang,Malaysia). pp.44-49

#### **Pranab Roy**, Rupam Bhattacharya, Hafizur Rahaman and Parthasarathi Dasgupta. “[A Best Path Selection Based Parallel Router For DMFBs](http://www.easychair.org/conferences/review_for_paper.cgi?a=t01cfa308731;paper=778109),” Proc. of IEEE International Symposium on Electronic Design ISED 2011,Kochi,India*,* pp.176-181.

#### Nachiketa Das, **Pranab Roy** and Hafizur Rahaman,”Runtime Congestion and Crosstalk Aware Router for FPGA Using Jbits3.0 for Partial Reconfigurable Application”, IEEE International Symposium on Electronic Design (ISED 2011) , pp.146-151.

#### **Pranab Roy**, Sukanta Roy, Hafizur Rahaman, and Parthasarathi Dasgupta, “A Novel Placement algorithm for Multi-pin Digital Microfluidic Biochips”, Proc. of *IEEE MWSCAS 2011,* pp 1-6

#### Nachiketa Das, **Pranab Roy**, and Hafizur Rahaman, “New Technique for Testing of Delay fault in Cluster Based FPGA”, , *IEEE MWSCAS 2011,* pp.1-4.

#### **Pranab Roy**, Hafizur Rahaman, and Parthasarathi Dasgupta, “Route Aware Placement Technique for Intelligent Collision Avoidance in Digital Microfluidic Biochips”, Proc. of *IEEE ASQED,Kualalampur,Malaysia, 2011,pp* 85-90

#### Nachiketa. Das,**Pranab Roy**,Parthasarathi Dasgupta and H. Rahaman, “Build-In-Self-Test of FPGA For Diagnosis of Delay Fault”, *IEEE ASQED 2011*, pp.54-59.

#### **Pranab Roy**, Hafizur Rahaman, and Parthasarathi Dasgupta, “A Group-Preferential Parallel-Routing Algorithm for Cross-referencing Digital Microfluidic Biochips*”, Proc. of IEEE/ACM ISVLSI Chennai,India,2011,* pp.317-318*.*

#### **Pranab Roy**, Hafizur Rahaman and Parthasarthi DasGupta “Hierarchical Multi-pin droplet routing in Digital Microfluidic Biochips with Intelligent Collision Avoidance”, Proc. of [ACM Great Lakes Symposium on VLSI 2011](http://www.informatik.uni-trier.de/~ley/db/conf/glvlsi/glvlsi2011.html#RoyRD11) (*GLSVLSI 2011*),Lausanne ,Switzerland, pp.229-234

#### Nachiketa Das, **Pranab Roy**, and Hafizur Rahaman, “On-Line Detection of Crosstalk Fault in FPGA Using BIST Model,” *VLSI Design and Test Symposium (VDAT 2011),* 2011.

#### **Pranab Roy**, Hafizur Rahaman and Parthasarthi DasGupta, “A Multipin droplet routing algorithm for Digital Microfluidic Biochips biodevices”, Proc. of INSTICC Biodevices, 2011 ,Rome,Italy,pp.217-223.

#### **Pranab Roy**, Hafizur Rahaman and Parthasarthi DasGupta, “A Novel Droplet Routing Algorithm for Digital Microfluidic Biochips”,Proc. of ACM/IEEE GLSVLSI ,Providance,USA,2010, pp.441-446.

#### **Pranab Roy**, Hafizur Rahaman and Parthasarthi DasGupta, , “Cluster Based Routing For Multi Pin Droplets In Digital Microfluidic Biochips with Intelligent Collision Avoidance”-Proc. of VLSI Design and Test Symposium(VDAT 2011),Pune,India,2011

####  Suman Bhattacharjee,Subhasree Bhattacharjee,Amit Konar and **Pranab Roy**, “Throughput Analysis for a Dynamic Spectrum Sharing Model with Finite Primary Users and Infinite secondary Users”, IEEE, ICCSIT, 2011, Chengdu,China.pp.636-640

#### Dipankar .Bhattacharya, B.Sarkar and **Pranab Roy**,“ Effect of template matching in vehicle number plate identification ”, IEEE,ICCSIT,2011,Chengdu,China

#### **Pranab Roy**, Tuhina Samanta, Hafizur Rahaman, Parthasarathi Dasgupta , “New Techniques for Droplet Routing in Digital Microfluidic Biochips”-Proc. of *VLSI Design and Test Symposium (VDAT 2010)* ,Chandigarh, India

#### N. Das, **Pranab Roy**, D. K. Das and H. Rahaman, “Feedback Bridging Fault Detection in Cluster Based FPGA by Using Muller-C Element”, IEEE ICFCC ,2009.

#### N. Das, **Pranab Roy**, and H. Rahaman, “On Line Testing of Single Feedback Bridging Fault in Cluster Based FPGA by Using Asynchronous Element”, proc. of IEEE International On-Line Testing Symposium 2008, pp.190-191

#### S. Ghosh, **Pranab Roy**, S. P. Maity and H. Rahaman, “Spread Spectrum Image Watermarking with Digital Design”, IEEE International Advance Computing Conference (IACC’09), March 6-7, 2009, India, pp. 2118-2123.

**Post Graduate Thesis Supervision**

1. Kaunaj Banerjee (Regn. No – 325417001)- “ Cyberphysical Implementation of Intelligent Traffic Control System” -2019- School of VLSI Technology, IIEST, Shibpur.
2. Subhankar Sarkar (Regn.No – 325417009)- “ Droplet Transportation in MEDA Based Biochips” -2019- School of VLSI Technology, IIEST, Shibpur.
3. Amiyo Sahoo(Regn. No –325416004) – “Development of schemes for prevention of cyberphysical attacks and Cyber Physical detection Architecture for medical Diagnostic applications using DMFB” - 2018– School of VLSI Technology , IIEST, Shibpur.
4. Binit Kumar Pandit ( Regn. No – 325416005)— “Development of algorithms for 3D IC Design and automation“— 2018– School of VLSI Technology , IIEST, Shibpur.
5. Avishek Ganguly (Regn. No -325416007) –“ Development of algorithms and VLSI architecture for embedded cyberphysical system application in intelligent traffic control systems “— 2018–-(in collaboration with Dr. Hafizur Rahaman) School of VLSI Technology , IIEST, Shibpur.
6. Saurav Kumar (Regn. No –325416008) –“ MEDA based biochip Architecture novel Testing and Routing Technique “ – 2018, School of VLSI Technology , IIEST, Shibpur.
7. Sandipan Haldar (Regn. No – 325415012) –“Development of algorithms for 3D IC design automation” – 2017-(in collaboration with Dr. Hafizur Rahaman) – School of VLSI Technology , IIEST, Shibpur.
8. Subhadip Haldar(Regn. No – 325415013) – “Testing techniques for MEDA Based Biochips ”– 2017– School of VLSI Technology , IIEST, Shibpur.
9. Ankita Pakhale(Regn. No –325415011) – “Cyberphysical Architecture for medical diagnostic applications using DMFB ” – 2017 – School of VLSI Technology , IIEST, Shibpur.
10. Poulomi Roy (Regn. No. 230812021) –“Development of testing technique of MEDA based Biochips ”- 2016 , School of IT – IIEST, Shibpur.
11. Debasish Saha Roy (Regn. No. 230812017) — “Intelligent traffic System: development of algorithms for dynamic Congestion Control” – 2016, Purabi Das School of IT – IIEST, Shibpur.
12. Subharajit Chakraborty (Regn. No. 230809038) – “ Layout based customozed testing technique for total microfluidic operations in Digital Microfluidic Biochips”- 2016, Purabi Das School of IT – IIEST, Shibpur.
13. Arko Dutt (Regn. No. - 235413015)– “Study and development of algorithms for 3-D integrated circuit design based on TSV optimization”–, 2016 (in collaboration with Dr. Hafizur Rahaman) – School of VLSI Technology , IIEST, Shibpur.
14. Sudeshna Chakraborty (Regn. No. – 235413004)–“ Development of techniques for sample preparation in Digital Microfluidic Biochips”–2016 School of VLSI Technology ,IIEST, Shibpur.
15. Anuradha Das Karmakar (Regn. No. - 235413003) –“Design of intelligent automated detection system for DMFBs”— 2016, School of VLSI Technology, IIEST, Shibpur.
16. Jayadrita Sarkar (Regn. No. - 235413009) – “Design of DMFBs: Development of design automation techniques and detector based architecture for Bioassay integration”- 2015 School of VLSI Technology – IIEST, Shibpur.
17. Ambuj Kumar (Regn. No – 235413010) –“Low Power ADC Design for Integration with microfluidic biochips ” (in collaboration with Prof. Manodepan Sahoo ) — 2015, School of VLSI Technology – IIEST, Shibpur.
18. Khokan Mondal(Regn. No – 235413006) – “Design of algorithm for Sample preparation, Architectural level and Geometrical level Synthesis of Digital Microfluidic Biochips ”— 2015,School of VLSI Technology – IIEST, Shibpur.
19. Swati Saha (Regn. No –230812003) – “Development of new wire planning technique for pin constrained digital microfluidic biochips” – 2015, Purabi Das School of IT – IIEST, Shibpur.
20. Nabanita Mahata ((Regn. No –230812004) – “ Study of the performance of Fused features of multi directional discriminent features of face recognition”- (in collaboration with Dr. Jamuna kanta Singh of Jadavpur University), 2015- Purabi Das School of IT – IIEST, Shibpur.
21. Ashapurna Mukherjee (Regn. No –230812024) – “Wash droplet optimization and routing using degree of contamination in digital microfluidic biochips ” –,2015 – Purabi Das School of IT – IIEST,Shibpur
22. Mayuri Kundu (Regn. No- 230812016)– “ Architecture level synthesis and sample preparation in DMFBs” –,2015 -- Purabi Das School of IT – IIEST, Shibpur.
23. Sutanu Haldar (Regn. No – 230809007) – “ Design of Algorithms for Synthesis and Placement in Digital Microfluidic Biochips” –2014 . Purabi Das School of IT – IIEST, Shibpur.
24. Samadrita Bhattacharya (Regn. No. –235412015) – “Development of algorithms for synthesis and wire planning in Digital Microfluidic Biochips”—2014, School of VLSI Technology, IIEST, Shibpur.
25. Aatreyi Bal (Regn. No- 235412021) – “Design of embedded systems for integrated operations in digital microfluidic biochips” –,2014, School of VLSI Technology, IIEST, Shibpur.
26. Moumita Goswami ( Regn. No – 230811023) – “Development of Algorithms for efficient placement and routing in Digital Microfluidic Biochips” – 2014, Purabi Das School of IT – IIEST, Shibpur.
27. Abir Sarkhel (Regn. No. -230811024)– “Development of customized and generalized Testing Algorithms in Digital microfluidic biochips ” –2014 . Purabi Das School of IT – IIEST, Shibpur.
28. Raja Dastidar (Regn. No. – 230811014) – “ Development of Architecture,Design Flow and simulation for ATDA based Biochip in 3D Platform”- 2014, Purabi Das School of IT – IIEST, Shibpur.
29. Firdousi Jamil Imam (Regn. No. – 230810002)— “ Study of droplet Routing and wire Planning in Digital Microfluidic Based Biochips”- 2014, Purabi Das School of IT – IIEST, Shibpur.
30. Tamosa Chakraborty(Regn. No – 230821006) – “Design of embedded systems for optical detection and analysis in Digital Microfluidic Biochips” –2014. Purabi Das School of IT – IIEST, Shibpur.
31. Akash Gupta(Regn. No – 230811031)- “ Genome Annotator Lite- An Annotation Pipeline System using Python, Perl and MySQL” – 2014, Purabi Das School of IT – IIEST, Shibpur.
32. Mahua Raha Patra (Regn. No. – 235411009) – “Embedded Architecture Design For Integration Of Multiple Biochips” –2013 , School of VLSI Technology, BESU, Shibpur.
33. Pampa Howladar (Regn. No- 235411019)– “Design automation of 3D Biochip” – 2013, School of VLSI Technology, BESU, Shibpur.
34. Somnath Chakraborty (Regn. No-230810035) – “Design of Algorithms for Detection forgery in Digital images”— 2013 – Purabi Das School of IT – BESU, Shibpur.
35. Nilanjana Bhowmik (Regn. No.- 230810009) — “ Physical design of DMFBs with Cross Contamination and Pin Constraint Optimization” – 2013 - Purabi Das School of IT, BESU, Shibpur.
36. Rupam Bhattacharya (Regn. No – 230809004) –“Design of Placement Simulator towards EDA Development for Digital Microfluidic Biochips ”— 2012 - Purabi Das School of IT, BESU, Shibpur.
37. Moudud Shohid (Regn. No. 235410008) – “Design of droplet analyzer and central processor for integration in DMFB”—2012 – School of VLSI Technology, BESU, Shibpur.
38. Sudipta Chakraborty(Regn. No –235410003) – “Development of algorithm and controller architecture for multiple bioassay scheduling and integration in DMFBs”—2012 – School of VLSI Technology, BESU, Shibpur.
39. Shatabdi Kar (Regn. No. - 235410006)– “Design of crosstalk aware routing and placement algorithm in FPGA.”— 2012 (in collaboration with Dr.Nachiketa Das )– School of VLSI Technology, BESU, Shibpur.
40. Bidisha Chowdhury (Regn. No.- 235306014) – “ design and Impelmentation of Advanced encryption standard architecture Using AES algorithm” – 2009, Purabi Das School of IT—BESU, Shibpur.
41. Swarnendu Kumar Chakraborty (Regn. No–235306024) – “Spectrum application by convolution coding with Viterbi Decoding” –2009, Purabi Das School of IT—BESU, Shibpur.

**PhD Supervision**

1. **Rupam Bhattacharya** – “Digital Microfluidic Biochips: Development of EDA Algorithms and design of Simulators” – Department of Information Technology, IIEST, Shibpur [completed -22nd August, 2019].
2. **Pampa Howladar** –“Techniques of Routing, Actuation, Threat Mitigation in MEDA based Digital Microfluidic Biochips” -Department of Information Technology, IIEST, Shibpur [submitted, 23rd September,2019 ].

**Awards**

1. Awarded Topper’s medal for coming **1st in M.Tech** (Information Technology) from B.E.S.U, Shibpur in 2008
2. Awarded gold medal for ranking **1st from** IEI, Kolkata section in **A.M.I.E**.-Section B in Electronics and Communication Engineering from IEI, Kolkata in 2001.
3. Received **best research paper** award in VLSI Design on Research Scholars day, 2014 by IIEST Research Scholar Day Committee.

**Professional Affiliations**

1. Corporate Member, Institution of Engineers, India (IEI) since 1993 (Membership No- AM-0758941-1).
2. Senior Member, Institute of Electrical and Electronics Engineers (IEEE) since 2012 (Membership No -92100224).
3. Associate Member ,Royal Institute of Naval Architects(RINA) ,UK since 2017 (membership No – 00402451).
4. Professional Member , Association for Computing Machinery(ACM) since 2018 (membership no – 5693421).

**Workshops/Trainings Organized**

1. Conducted a summer course on “VLSI design” at B.E.S.U, Shibpur as

 Course coordinator held from 23rd June, 2010 to 31st July, 2010 on behalf

 of School of VLSI Technology in collaboration with M/S Metalogic Systems

 Private Limited.

1. Conducted summer training Two weeks course on “Analog design using cadence tools” as Course coordinator held on May, 2013 at School of VLSI Technology, BESU, Shibpur.

**List of Seminars/Conferences/Workshops attended/presented**

1. Workshop on Xilinx FPGA– I.I.T, Kharagpur , 27th Feb– 3rd March,2007
2. 11th International symposium of VLSI design and test – Saha Institute of Nuclear Physics , Kolkata , 5th – 11th August,2007.
3. Training program on Mentor Graphics EDA Tools – I.I.Sc, Bangalore , 27th Aug – 1st Sept,2007.
4. 21st IEEE International conference on VLSI design – Hyderabad, 4th -8th January, 2008.
5. Training program on Synopsys EDA Tools - I.I.Sc, Bangalore , 31st Mar – 4th Apr, 2008
6. Cadence Vendor Training program - I.I.Sc, Bangalore, 21st – 27th April, 2008.
7. Challenges in VLSI design: Cutting edge perspective(Invited talk)- – Dept. of IT and School of VLSI Tech, BESU, Shibpur, 21st – 25th July,2008.
8. Workshop on “ Linux system administration and documentation using Latex “ – Dept. of Electrical Engg, BESU,Shibpur , 18th – 24th December,2008.
9. National workshop on “Recent trends in VLSI Design and Microelectronics “- Dept. of ETC, BESU, Shibpur, 4th -10th January,2009.
10. 2nd national workshop on Nanoscience and Biochips – Indian Statistical Institute ,Kolkata, 16-17 Feb ,2009.
11. Open Source Workshop – Dept. of IT, BESU, Shibpur, 27th – 29th July,2009.
12. Workshop on Emerging Technology in Computing (Invited speaker) – St. Thomas' College of Engg. & Tech., Kolkata, 6th – 11th June,2011.
13. IEEE Computer Society annual Symposium on VLSI Design (ISVLSI) (Poster presentation)- - IIT, Madras, Chennai, India, 4th -6th July,2011.
14. 15th VLSI Design and Test Symposium (oral presentation)- - Pune,India,7th -9th July,2011.
15. IEEE International Conference on Biomedical Engineering(oral presentation)- - Penang, Malaysia ,27th -28th February,2012.
16. IEEE 2nd International conference on Informatics ,Electronics and Vision ,2012 (oral presentation)- Dhaka,Bangladesh.18th – 19th May,2012.
17. 16th International Symposium of VLSI Design and Test – BESU, Shibpur ,1st – 4th July,2012
18. IEEE International conference on Communication, Devices and Intelligent Systems (CODIS) (oral presentation) - Jadavpur University, Kolkata, 28th -29th December, 2012
19. IEEE 7th International Design and Test Symposium (oral presentation)- - Doha, Qatar ,15th -17th December,2012
20. Research Scholar’s Day – BESU, Shibpur, 29th -30th January,2013.
21. Seminar on Computing and Informatics (Invited Speaker) - St. Thomas' College of Engg. & Tech., Kolkata, 11th -14th June,2013.
22. 17th VLSI Design and Test Symposium (oral presentation)- Jaipur, India 27th -30th July,2013.
23. A research promotion workshop on “Signal processing and wireless communication” – Dept. of IT, BESU, Shibpur ,22nd -24th August,2013.
24. 4th IEEE International Symposium of Electronic System Design(oral presentation)- -Nanyang Technological University ,Singapore, 12th -13th December2013.
25. 1st IEEE International Conference on Control, Automation, Robotics and Embedded systems (oral presentation)- Jabalpur, India ,16th -18th December,2013.
26. 27th IEEE International conference of VLSI Design (oral presentation)- - Indian Institute of Technology, Mumbai, India, 5th -9th January, 2014.
27. Workshop on “Emerging and post CMOS Technologies” – Dept. of IT, IIEST, Shibpur, 16th – 18th June ,2014.
28. Workshop on Nanotechnology and biochips – Dept. of CST, IIEST, Shibpur, 1st – 3rd July, 2014.
29. 5th International conference on Electronic system design (oral presentation)- – NIT, Suratkal, 15th – 17th December,2014.
30. 7th workshop on Nano electronics and Biochips (Invited talk)- – ISI, Kolkata, 18th -19th March,2014.
31. LABVIEW core 1 and core 2 training by NI Systems India Pvt. Ltd. – IIEST, Shibpur , 19th -23rd January,2015
32. Testing and Design for testability for digital integrated circuits (GIAN Initiative) – IIEST, Shibpur ,25th July – 5th Aug,2016.
33. Workshop on Digital VLSI  Design (Invited speaker) – Bankura Unnayani Institute of Engineering, Bankura, 20th – 24th September,2016.
34. Short term course on “ Advanced wireless sensor network “ – Dept of IT, IIEST, Shibpur, 26th – 29th September,2016
35. Seminar on “ Recent trends in wireless communication and sensor networks “ – Dept. of ETC, IIEST, Shibpur , 3-5th October,2016.
36. Refresher course on VLSI design and Nanotechnology issues and challenges (invited speaker) – Jadavpur University, 28th November – 17th December, 2016.
37. Seminar on “Information security “– Dept. of IT, IIEST, Shibpur, 9-11th February, 2017.
38. 7th IEEE International Symposium on Embedded Computing and Systems Design, 2017,Durgapur, India,19-20 th December,2017.
39. 1st IEEE International Symposium on Devices, Circuits and Systems, 2018, IIEST, Shibpur, India, 29-31st March, 2018.
40. Course on “Testing of 3D Integrated Circuits” – Under SPARC project-“ Design for test solution for 3D Integrated Circuits” ,2019,IIEST,Shibpur,India , 19th June 2019 – 12th July,2019.

**Computer Proficiencies**

* + **Programming Languages** - Core JAVA, J2EE, C, C++, Python.
	+ **Modelling Languages** - UML (Rational Rose).
	+ **DBMS** – Oracle 9 i and 10G, MySQL.
	+ **Operating Systems** – Windows, Linux.
	+ **Hardware Description Language** – VHDL , Verilog
	+ **EDA Tools** – Xilinx FPGA, Synopsys EDA Tools and Cadence EDA Tools.

**Personal Details**

Date of Birth – 14th November, 1966.

Place of Birth – Kolkata, West Bengal, India.

Gender – Male

Nationality – Indian.

Father’s Name – Jyotsna Moy Roy (Late).

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I hereby declare that the statements made by me are true, complete and correct to the best of my knowledge and belief.

***Signature***

**Date** – 3rd October**, 2019**

**Place** – Kolkata